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Search: L4

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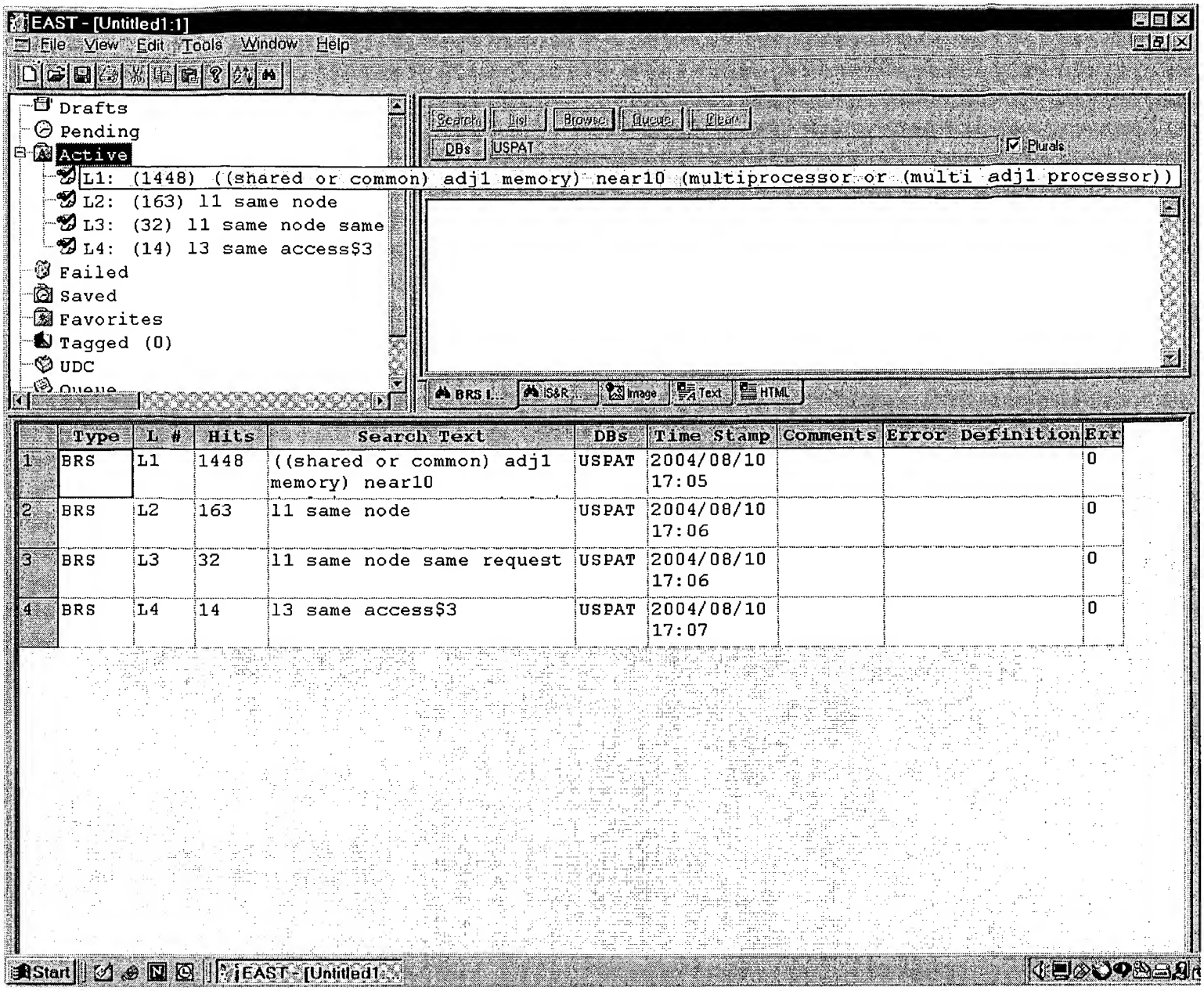
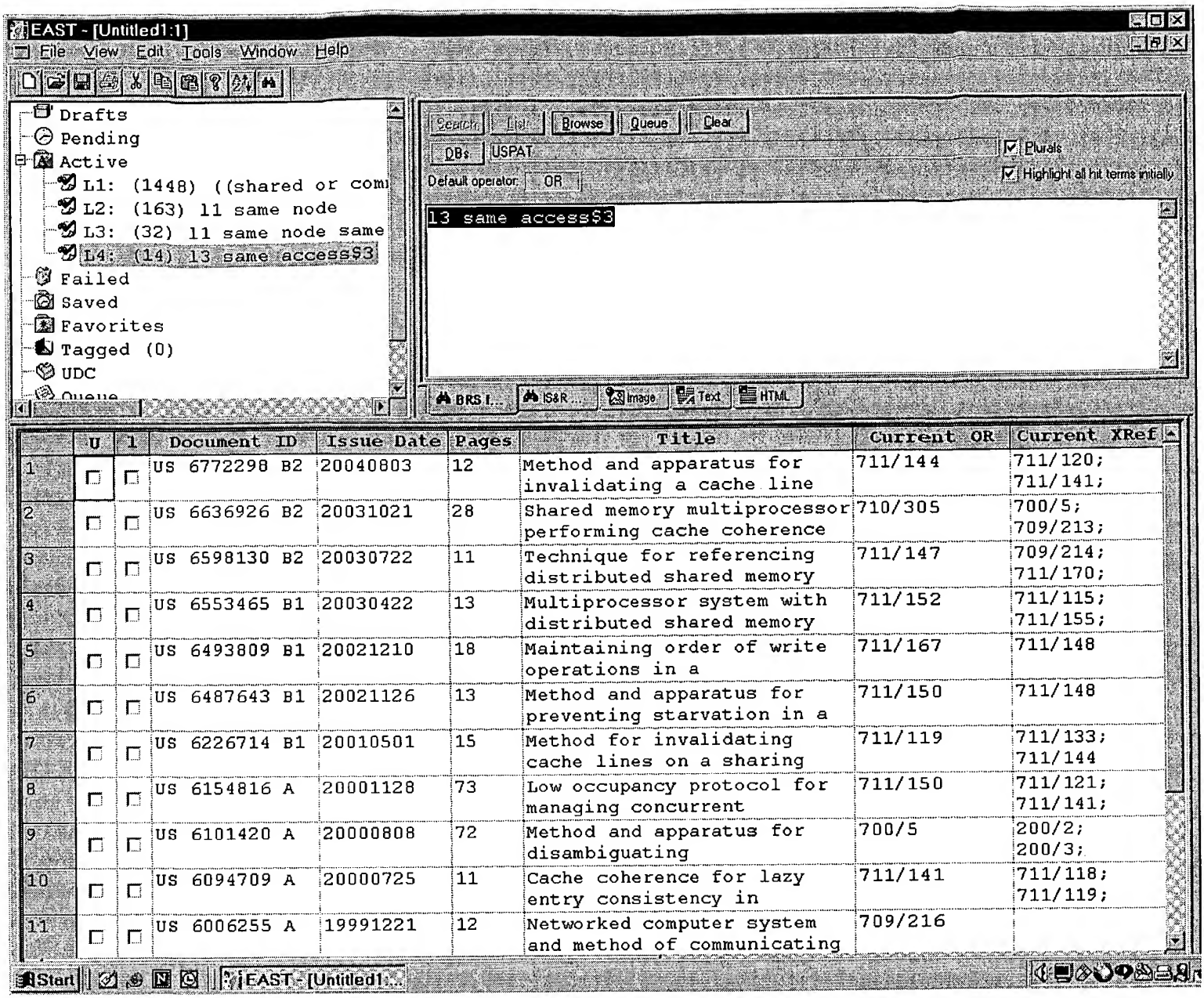
	DB=USPT,USOC; PLUR=YES; OP=OR		
L4	l1 and L3	16	L4
L3	L2 near10 cache	46	L3
L2	((shared or common) adj1 memory) near10 (multprocessor or (multi adj1 processor))	352	L2
L1	710/305,317,300,62,4,72;711/141,148,120;709/213,214,251;700/5;712/14,211.ccls.	4434	L1

END OF SEARCH HISTORY



	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	1448	((shared or common) adj1 memory) near10	USPAT	2004/08/10 17:05			0
2	BRS	L2	163	l1 same node	USPAT	2004/08/10 17:06			0
3	BRS	L3	32	l1 same node same request	USPAT	2004/08/10 17:06			0
4	BRS	L4	14	l3 same access$3	USPAT	2004/08/10 17:07			0



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6772298 B2	20040803	12	Method and apparatus for invalidating a cache line	711/144	711/120; 711/141;
2	☐	☐	US 6636926 B2	20031021	28	Shared memory multiprocessor performing cache coherence	710/305	700/5; 709/213;
3	☐	☐	US 6598130 B2	20030722	11	Technique for referencing distributed shared memory	711/147	709/214; 711/170;
4	☐	☐	US 6553465 B1	20030422	13	Multiprocessor system with distributed shared memory	711/152	711/115; 711/155;
5	☐	☐	US 6493809 B1	20021210	18	Maintaining order of write operations in a	711/167	711/148
6	☐	☐	US 6487643 B1	20021126	13	Method and apparatus for preventing starvation in a	711/150	711/148
7	☐	☐	US 6226714 B1	20010501	15	Method for invalidating cache lines on a sharing	711/119	711/133; 711/144
8	☐	☐	US 6154816 A	20001128	73	Low occupancy protocol for managing concurrent	711/150	711/121; 711/141;
9	☐	☐	US 6101420 A	20000808	72	Method and apparatus for disambiguating	700/5	200/2; 200/3;
10	☐	☐	US 6094709 A	20000725	11	Cache coherence for lazy entry consistency in	711/141	711/118; 711/119;
11	☐	☐	US 6006255 A	19991221	12	Networked computer system and method of communicating	709/216	

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(shared or common) and memory<and>multiprocess Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **The impact of negative acknowledgments in shared memory scienti applications**
Mainak Chaudhuri; Heinrich, M.;
Parallel and Distributed Systems, IEEE Transactions on , Volume: 15 , Issue: 2 , Feb 2004
Pages:134 - 150

[Abstract] [PDF Full-Text (1831 KB)] **IEEE JNL**

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2 **A DSM architecture for a parallel computer Cenju-4**
Hosomi, T.; Kanoh, Y.; Nakamura, M.; Hirose, T.;
High-Performance Computer Architecture, 2000. HPCA-6. Proceedings. Sixth International Symposium on , 8-12 Jan. 2000
Pages:287 - 298

[Abstract] [PDF Full-Text (384 KB)] **IEEE CNF**

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3 **The effect of limited network bandwidth and its utilization by laten hiding techniques in large-scale shared memory systems**
Sunil Kim; Veidenbaum, A.V.;
Parallel Architectures and Compilation Techniques., 1997. Proceedings. 1997 International Conference on , 10-14 Nov. 1997
Pages:40 - 51

[Abstract] [PDF Full-Text (1284 KB)] **IEEE CNF**

---

4 **Performance evaluation of a WDMA OIDSM multiprocessors**
I-Shyan Hwang;
Parallel and Distributed Systems, 1996. Proceedings., 1996 International Conference on , 3-6 June 1996

Pages:162 - 168

[Abstract] [PDF Full-Text (556 KB)] **IEEE CNF**

5 **Computation/communication balance-point modeling in multiproce**
Hamacher, V.C.;
Communications, Computers and Signal Processing, 1999 IEEE Pacific Rim Conference on , 22-24 Aug. 1999
Pages:141 - 144

[Abstract] [PDF Full-Text (380 KB)] **IEEE CNF**

6 **Performance evaluation of cache depot on CC-NUMA multiprocesso**
Hung-Chang Hsiao; Chung-Ta King;
Parallel and Distributed Systems, 1998. Proceedings., 1998 International Conference on , 14-16 Dec. 1998
Pages:519 - 526

[Abstract] [PDF Full-Text (204 KB)] **IEEE CNF**

7 **The performance impact of false subpage sharing in KSR1**
Cukic, B.; Bastani, F.B.;
Frontiers of Massively Parallel Computation, 1995. Proceedings. 'Frontiers '95 Fifth Symposium on the , 6-9 Feb. 1995
Pages:64 - 71

[Abstract] [PDF Full-Text (560 KB)] **IEEE CNF**

Performance evaluation of cache depot on CC-NUMA multiprocessors

Hung-Chang Hsiao Chung-Ta King
Dept. of Comput. Sci., Nat. Tsing Hua Univ., Hsinchu, Taiwan;

This paper appears in: **Parallel and Distributed Systems, 1998. Proceedings., 1998 International Conference on**

Meeting Date: 12/14/1998 - 12/16/1998
Publication Date: 14-16 Dec. 1998
Location: Tainan Taiwan
On page(s): 519 - 526
Reference Cited: 15
Number of Pages: xxi+826
Inspec Accession Number: 6135775

Abstract:
Cache depot is a performance enhancement technique on **cache**-coherent non-uniform **memory** access (CC-NUMA) **multiprocessors**, in which **nodes** in the system store extra **memory** blocks on behalf of other **nodes**. In this way **memory requests** from a **node** can be satisfied by nearby depot **nodes** without going all the way to the home **node**. This not only reduces **memory** access latency and network traffic, but also spreads the network load more evenly. We study the design strategy for **cache** depot that: enhances

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the network interface of each **node** to include a depot **cache**, which stores those extra **memory** blocks for other **nodes**; and employs a new multicast routing scheme, which is called the multi-hop worms and works cooperatively with depot **caches**, to transmit coherence messages. By considering message routing and depot **caches** together the design concept can be applied even to those CC-NUMA systems that have a non-hierarchical, scalable interconnection network. We have developed an execution-driven simulator to evaluate the effectiveness of the design strategy. Performance results from using four SPLASH-2 benchmarks show that the design strategy improves the performance of the CC-NUMA **multiprocessor** by 11% to 21%. We have also studied in depth various factors which affect the performance of **cache** depot

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Index Terms:

cache storage data integrity distributed **shared memory** systems message passing multicast communication performance evaluation storage management CC-NUMA **multiprocessors** SPLASH-2 benchmarks **cache** depot **cache**-coherent non-uniform **memory** access coherence messages execution-driven simulator **memory** access latency **memory** blocks message routing multi-hop worms multicast routing scheme network interface network load network traffic performance enhancement technique performance evaluation scalable interconnection network

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Computation/communication balance-point modeling in multiprocessors

Hamacher, V.C.
Dept. of Electr. & Comput. Eng., Queen's Univ., Kingston, Ont., Canada;

This paper appears in: **Communications, Computers and Signal Processing, 1999 IEEE Pacific Rim Conference on**

Meeting Date: 08/22/1999 - 08/24/1999
Publication Date: 22-24 Aug. 1999
Location: Victoria, BC Canada
On page(s): 141 - 144
Reference Cited: 5
Number of Pages: xv+618
Inspec Accession Number: 6497422

Abstract:
An analytic model for predicting processor utilization in a CC-NUMA (**cache** coherent non-uniform **memory** access) **shared-memory multiprocessor** is developed. The interconnection network in such systems transfers **cache** line messages between processor **caches** and **memory** modules on read and write misses. The major component of the miss penalty, for the case of large systems, is the network delay. Using only a relatively small number of **node** parameters (**cache** miss rate, **cache** line length,

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number of outstanding transfer **requests** allowed, **memory** access time, proportion of Reads to Writes), along with the bandwidth and delay versus throughput characteristics of the network, the analytic model is shown to give good estimates of the processor utilization values derived from an independent detailed simulation study. In particular, for **multiprocessor** sizes of 72 and 108 **nodes**, and for variations in the **node** parameters, the processor utilization values determined by the analytic model are within 10% of the simulation results. Processor utilizations vary from 0.41 to 0.88. The interconnection network involved is a hierarchical slotted-ring system

Index Terms:

multiprocessor interconnection networks **shared memory** systems CC-NUMA **shared-memory** **multiprocessor** analytic model bandwidth **cache** line message transfer computation/communication balance-point modeling hierarchical slotted-ring system interconnection network **memory** module miss penalty **multiprocessors** network delay **node** parameters processor **caches** processor utilization prediction read and write misses throughput characteristics

Documents that cite this document

There are no citing documents available in IEEE Xplore at this time.

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L4: Entry 2 of 15 File: USPT May 18, 2004

DOCUMENT-IDENTIFIER: US 6738870 B2
TITLE: High speed remote storage controller

Abstract Text (1):
A high speed remote storage controller system for a computer system has cluster nodes of symmetric multiprocessors. A plurality of clusters of symmetric multiprocessors each of has a plurality of processors, a shared cache memory, a plurality of I/O adapters and a main memory accessible from the cluster. Each cluster has an interface for passing data between cluster nodes of the symmetric multiprocessor system. Each cluster has a local interface and interface controller. The system provides one or more remote storage controllers each having a local interface controller and a local-to-remote data bus. A remote resource manager manages the interface between clusters of symmetric multiprocessors. The remote store controller is responsible for processing data accesses across a plurality of clusters and processes data storage operations involving shared memory. A macro is provided for processing a plurality of simultaneous data storage operations either synchronously through interaction with a sequential multistage centralized pipeline to serialize requests and provide address interlocking services or asynchronously whereby main memory accesses bypass a centralized system pipeline. These accesses can occur in parallel with other remote storage operations.

CLAIMS:

1. A high speed remote storage controller system for a computer system having cluster nodes of symmetric multiprocessors, comprising one or more remote storage controllers each having an associated local interface controller, and a local-to-remote data bus, and the one or more remote storage controllers responsive to a remote management system for managing the resources comprising the remote storage controller for data accesses between clusters of symmetric multiprocessors which are controlled for inter nodal storage operations by one of said remote storage controller system, each of which clusters has a plurality of processors, a shared cache memory, a plurality of I/O adapters and a main memory accessible from the cluster, said remote store controller while processing data accesses across a plurality of clusters for data storage operations involving shared memory and inter nodal storage operations, enlisting a single one of said remote storage controller to perform remote cast outs, store requests from an I/O adapter, main storage padding operations, and main memory move page operations and while performing remote data storage operations to main memory, said enlisted single remote storage controller also handles cross cluster invalidations associated with maintaining inter-nodal cache coherency for said computer system having cluster nodes of symmetric multiprocessors, and which contains a deadlock avoidance mechanism designed to detect inter-nodal deadlocks which normally result from one resource on a local cluster waiting for a second resource on a remote cluster which is deadlocked against a third resource on said remote cluster waiting for a fourth resource on the local cluster which is deadlocked against said first resource on the local cluster, and which employs a fast hang quiesce mechanism embedded in each remote storage resource which works in conjunction with similar fast hang quiesce mechanisms throughout the System Controller to prevent system-wide hangs either caused by the failure of the current remote storage resource to make forward progress or by the failure of another operation somewhere in the Storage Controller

to make forward progress.

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L4: Entry 2 of 15 File: USPT May 18, 2004

US-PAT-NO: 6738870
DOCUMENT-IDENTIFIER: US 6738870 B2

TITLE: High speed remote storage controller

DATE-ISSUED: May 18, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Van Huben; Gary A.	Poughkeepsie	NY		
Blake; Michael A.	Wappingers Falls	NY		
Mak; Pak-Kin	Poughkeepsie	NY		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 09/ 745593 [PALM]
DATE FILED: December 22, 2000

PARENT-CASE:
RELATED APPLICATIONS This application entitled "High Speed Remote Storage Controller" is related to U.S. Ser. No. 09/745,830, filed Dec. 22, 2003 and entitled "Method for deadlock avoidance in a cluster environment"; and also to U.S. Ser. No. 09/747,686, filed Dec. 22, 2003, and entitled "Clustered Computer System with Deadlock Avoidance". These co-pending applications and the present application are owned by one and the same assignee, International Business Machines Corporation of Armonk, N.Y. The descriptions set forth in these co-pending applications are hereby incorporated into the present application by this reference. Trademarks: S/390 and IBM are registered trademarks of International Business Machines Corporation, Armonk, N.Y., U.S.A. Other names such as z900 may be registered trademarks or product names of International Business Machines Corporation or other companies.

INT-CL: [07] G06 F 12/00

US-CL-ISSUED: 711/150; 711/124, 711/130, 711/147, 711/148
US-CL-CURRENT: 711/150; 711/124, 711/130, 711/147, 711/148

FIELD-OF-SEARCH: 711/124, 711/130, 711/148, 711/147, 711/150, 709/214

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

h e b b g e e e f c e e ge

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	6108753	August 2000	Bossen et al.	711/118
☐	6175905	January 2001	Manning	711/169

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
945798	September 1999	EP	

OTHER PUBLICATIONS

Store Pad (Clear Line) Service Mechanism, IBM Technical Disclosure Bulletin, Apr. 1983, vol. 25, No. 11A, pp. 5893-5841.*
Multiprocessing System Memory Access Queue and Scheduling Apparatus, IBM Technical Disclosure Bulletin, May 1992, vol. 34, No. 12, pp. 299-300.*
Jim Handy, The Cache Memory Book, 1998, Academic Press, pp. 72-75.*
IBM PPC403GCX Embedded Controllers User's Manual, May 1998, IBM Coporation, pp. 4-1 to 4-3.

ART-UNIT: 2188

PRIMARY-EXAMINER: Padmanabhan; Mano

ASSISTANT-EXAMINER: Ross; John M

ATTY-AGENT-FIRM: Augspurger; Lynn L.

ABSTRACT:

A high speed remote storage controller system for a computer system has cluster nodes of symmetric multiprocessors. A plurality of clusters of symmetric multiprocessors each of has a plurality of processors, a shared cache memory, a plurality of I/O adapters and a main memory accessible from the cluster. Each cluster has an interface for passing data between cluster nodes of the symmetric multiprocessor system. Each cluster has a local interface and interface controller. The system provides one or more remote storage controllers each having a local interface controller and a local-to-remote data bus. A remote resource manager manages the interface between clusters of symmetric multiprocessors. The remote store controller is responsible for processing data accesses across a plurality of clusters and processes data storage operations involving shared memory. A macro is provided for processing a plurality of simultaneous data storage operations either synchronously through interaction with a sequential multistage centralized pipeline to serialize requests and provide address interlocking services or asynchronously whereby main memory accesses bypass a centralized system pipeline. These accesses can occur in parallel with other remote storage operations.

4 Claims, 10 Drawing figures

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L4: Entry 4 of 15 File: USPT Nov 11, 2003

DOCUMENT-IDENTIFIER: US 6647453 B1
TITLE: System and method for providing forward progress and avoiding starvation and livelock in a multiprocessor computer system

Brief Summary Text (14):
Briefly, the invention relates to a system and method for avoiding "livelock" and "starvation" among two or more input/output (I/O) devices competing for the same data in a symmetrical multiprocessor (SMP) computer system. The SMP computer system includes a plurality of interconnected processors having corresponding caches, one or more memories that are shared by the processors, and a plurality of I/O bridges to which the I/O devices are coupled. Each I/O bridge includes one or more upstream buffers and one or more downstream buffers. An up engine is coupled to the upstream buffer and is controls the flow of information, including requests for data, from the I/O devices to the processors and shared memory. A down engine is coupled to the downstream buffer, and controls the flow of information from the processors and shared memory to the I/O devices. A cache coherency protocol is executed in the I/O bridge in order to keep the data in the downstream buffer coherent with the processor caches and shared memory. As part of the cache coherency protocol, the I/O bridge obtains "exclusive" (not shared) ownership of all data fetched from the processor caches and the shared memory, and invalidates and releases any data in the downstream buffer that is requested by a processor or by some other I/O bridge.

L4: Entry 4 of 15 File: USPT Nov 11, 2003

US-PAT-NO: 6647453
DOCUMENT-IDENTIFIER: US 6647453 B1

TITLE: System and method for providing forward progress and avoiding starvation and livelock in a multiprocessor computer system

DATE-ISSUED: November 11, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Duncan; Samuel H.	Arlington	MA		
Ho; Steven	Westford	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Development Company, L.P.	Houston	TX			02

APPL-NO: 09/ 652984 [PALM]
DATE FILED: August 31, 2000

PARENT-CASE:
INCORPORATION BY REFERENCE OF RELATED APPLICATIONS This patent application is related to the following co-pending, commonly owned U.S. Patent Applications, all of which were filed on even date with the within application for United States Patent and are each hereby incorporated by reference in their entirety: U.S. patent application Ser. No. 09/652,644 entitled ADAPTIVE DATA PREFETCH PREDICTION ALGORITHM; U.S. patent application Ser. No. 09/653,133 entitled UNIQUE METHOD OF REDUCING LOSSES IN CIRCUITS USING V.sup.2 PWM CONTROL; U.S. patent application Ser. No. 09/652,641 entitled IO SPEED AND LENGTH PROGRAMMABLE WITH BUS POPULATION; U.S. patent application Ser. No. 09/652,458 entitled PARTITION FORMATION USING MICROPROCESSORS IN A MULTIPROCESSOR COMPUTER SYSTEM; U.S. Provisional Patent Application Ser. No. 60/304,167 entitled SYSTEM AND METHOD FOR USING FUNCTION NUMBERS TO INCREASE THE COUNT OF OUTSTANDING SPLIT TRANSACTIONS; U.S. patent application Ser. No. 09/653,180 entitled ONLINE ADD/REMOVAL OF SERVER MANAGEMENT INFRASTRUCTURE; U.S. patent application Ser. No. 09/652,494 entitled AUTOMATED BACKPLANE CABLE CONNECTION IDENTIFICATION SYSTEM AND METHOD; U.S. patent application Ser. No. 09/652,459 entitled CLOCK FORWARDING DATA RECOVERY; U.S. patent application Ser. No. 09/652,980 entitled CLOCK FORWARD INITIALIZATION AND RESET SIGNALING TECHNIQUE; U.S. patent application Ser. No. 09/944,515 entitled PASSIVE RELEASE AVOIDANCE TECHNIQUE; U.S. patent application Ser. No. 09/652,985 entitled COHERENT TRANSLATION LOOK-ASIDE BUFFER; U.S. patent application Ser. No. 09/652,645 entitled DETERMINISTIC HARDWARE BEHAVIOR BETWEEN MULTIPLE ASYNCHRONOUS CLOCK DOMAINS THROUGH THE NOVEL USE OF A PLL; and U.S. patent application Ser. No. 09/655,171 entitled VIRTUAL TIME OF YEAR CLOCK.

INT-CL: [07] G06 F 13/36, G06 F 13/00, G06 F 12/00

US-CL-ISSUED: 710/306; 710/100, 710/104, 710/300, 710/310, 711/141
US-CL-CURRENT: 710/306; 710/100, 710/104, 710/300, 710/310, 711/141

FIELD-OF-SEARCH: 710/100, 710/300, 710/104, 710/306, 710/310, 711/141

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5515523	May 1996	Kalkunte et al.	
☐	5625779	April 1997	Solomon et al.	
☐	5884100	March 1999	Normoyle et al.	
☐	6014690	January 2000	VanDoren et al.	
☐	6035376	March 2000	James	711/145
☐	6078997	June 2000	Young et al.	711/144
☐	6094686	July 2000	Sharma	
☐	6247102	June 2001	Chin et al.	
☐	6389526	May 2002	Keller et al.	712/30

OTHER PUBLICATIONS

Chapter 3 Memory Management, http://www.linuxdoc.org/LDP/tlk/mm/memory.html, (c) 1996-1999, pp. 1-23.
Multiprocessors (7 pages).
Russo, Andrew P., The AlphaServer 2100 I/O Subsystem, http://www.digital.com, (c) 1994, pp. 1-13.
Duncan, Samuel H., Keefer, Craig D., McLaughlin, Thomas A., High Performance I/O Design in the AlphaServer 4100 Symmetric Multiprocessing System, Compaq Digital Technical Jounrnal, pp. 1-24.
Steinman, Maurice B., Harris, George J., Kocev, Andrej, Lamere, Virginia C. and Pannell, Roger D., The AlphaServer 4100 Cached Processor Module Architecture and Design, Digital Technical Journal, pp. 1-29.
Bannon, Peter, Alpha 21364: A Scalable Single-chip SMP, (c) 1999, pp. 1-4.
New Compaq AlphaServer GS Series Architecture White Paper, Compaq Computer Corporation, (c)2000, pp. 1-11.

ART-UNIT: 2181

PRIMARY-EXAMINER: Vo; Tim

ABSTRACT:

A system and method avoids "livelock" and "starvation" among two or more input/output (I/O) devices of a symmetrical multiprocessor (SMP) computer system competing for the same data. The SMP computer system includes a plurality of interconnected processors, one or more memories that are shared by the processors, and a plurality of I/O bridges to which the I/O devices are coupled. A cache coherency protocol is executed the I/O bridges, which requires the I/O bridges to

obtain "exclusive" (not shared) ownership of all data stored by the bridges. In response to a request for data currently stored by an I/O bridge, the bridge first copies at least a portion of that data to a non-coherent buffer before invalidating the data. The bridge then takes the largest amount of the data saved in its non-coherent buffer that its knows to be coherent, and releases only that known coherent amount to the I/O device, and then discards all of the saved data.

11 Claims, 11 Drawing figures

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L4: Entry 5 of 15 File: USPT Oct 21, 2003

DOCUMENT-IDENTIFIER: US 6636926 B2
TITLE: Shared memory multiprocessor performing cache coherence control and node controller therefor

Brief Summary Text (9):
The system according to the second reference described above, in which each node is not configured only with a processor having a cache memory, is a multiprocessor system in which each node is configured with a processor including a cache memory, a memory and an I/O device. This system is what is called a distributed shared memory multiprocessor (physically-distributed logically-shared memory multiprocessor), in which the memories and the I/O devices are distributed physically among the nodes but shared logically by the nodes. In the system according to the second reference, a plurality of nodes are coupled to each other by buses for address and coupled by a crossbar switch for data. By use of four address buses, four address snoop operations can be performed in parallel. The physical address space is divided into four parts so that each address bus can snoop different address spaces at the same time.

CLAIMS:

1. A shared memory multiprocessor comprising: a plurality of nodes each configured with at least one of a processor having a cache memory, a memory device and an I/O device, and a node controller; and an inter-node connection network for interconnecting a plurality of said nodes; wherein at least one of a plurality of said nodes includes said processor and at least one of said memory device and said I/O device, and the whole of a plurality of said nodes include at least one said processor, at least one said memory device and at least one said I/O device; wherein said node controller of each of a plurality of said nodes includes a processor unit constituting an interface with said processor in a local node, at least a memory unit constituting an interface with said memory device in the local node and an I/O unit constituting an interface with said I/O device in the local node, a network unit constituting an interface with said inter-node connection network, and an intra-node connection circuit for connecting said processor unit and at least one of said memory device and said I/O device to said inter-node connection network unit; wherein said processor unit includes an inter-unit address decode circuit and a cache coherence control circuit, said inter-unit address decode circuit decoding the control information and the address information in a memory access request or an I/O access request issued by the processor in the local node, and adding to said access request the information on the node associated with the memory unit or the I/O unit intended as a destination of said access request, the information on the unit intended as a destination of said access request, and the cache coherence control information indicating whether the cache coherence control is required or not, said cache coherence control circuit performing the cache coherence control of the processor in the local node in the case where the cache coherence control information added to the access request received from said network unit indicates that the cache coherence control is required; wherein said I/O unit includes an inter-unit address decode circuit whereby the node information and the unit information for the memory unit or the I/O unit intended as a access request destination and the cache coherence control information indicating whether the cache coherence control is required or not are added to the memory access

request or the I/O access request issued by the I/O device in the local node; wherein said network unit includes a transfer unit for transferring the access request received from said intra-node connection circuit to said inter-node connection network, and a transfer unit for transferring the access request transferred thereto from said inter-node connection network to said intra-node connection network; wherein said intra-node connection circuit transfers said access request to the unit in the local node designated as a destination of transfer based on the cache coherence control information, the node information and the unit information added to the access request transferred from said inter-node connection network through said network unit; and wherein said inter-node connection network transfers said access request to the node designated by the cache coherence control information and the node information added to the access request received from said network unit.

6. A shared memory multiprocessor comprising: a plurality of nodes each configured with at least one of a processor having a cache memory, a memory device and an I/O device, and a node controller; and an inter-node connection network for interconnecting a plurality of said nodes; wherein at least one of a plurality of said nodes includes said processor and at least one each of said memory device and said I/O device, and the whole of a plurality of said nodes include at least one said processor, at least one said memory device and at least one said I/O device; wherein said node controller of each of a plurality of said nodes includes a processor unit constituting an interface with said processor in the local node, a memory unit constituting an interface with said memory device in the local node and/or an I/O unit constituting an interface with said I/O device in the local node, a network unit constituting an interface with said inter-node connection network, and an intra-node connection circuit for connecting said processor unit, at least one of said memory device and said I/O device, and said network unit; wherein said processor unit includes an inter-unit address decode circuit and a cache coherence control circuit, said inter-unit address decode circuit decoding the control information and the address information in said access request, and operating in such a manner that the information on the node associated with the memory unit or the I/O unit intended as an access request destination, the information on the unit intended as an access request destination, and the cache coherence control information indicating whether the cache coherence control is required or not, are added to a memory access request or an I/O access request issued by the processor in the local node, said cache coherence control unit performing the cache coherence control of the processor in the local node in the case where the cache coherence control information added to the access request received from said network unit indicates that the cache coherence control is required,; wherein said I/O unit includes an inter-unit address decode circuit for adding the node information and the unit information for the memory unit or the I/O unit intended as an access request destination and the cache coherence control information indicating whether the cache coherence control is required or not, to the memory access request or the I/O access request issued by the I/O device in the local node; wherein said network unit includes a transfer unit for transferring the access request received from said intra-node connection circuit to said inter-node connection network, and a transfer unit for transferring the access request transferred thereto from said inter-node connection network to said intra-node connection network; wherein said intra-node connection circuit operates in such a manner that in the case where a unit in the local node is designated as the destination of transfer based on the cache coherence control information, the node information and the unit information added to the access request transferred from said inter-node connection network through said network unit, said access request is transferred to the unit designated as the transfer destination; wherein said intra-node connection circuit includes a unit designation circuit for designating the destination of transfer of said access request based on the cache coherence control information, the node information and the unit information added to the access request transferred from said inter-node connection network, and a transfer unit for transferring said access request to the unit connected to said intra-node

connection circuit in response to the designation of said unit designation circuit; wherein said inter-node connection network includes a node designation circuit for designating the destination of transfer of said access request based on the cache coherence control information, the node information and the unit information added to the access request sent out from said network unit, and a transfer unit for transferring said access request in response to the designation of said node designation circuit; and wherein that access request issued by said processor or said I/O device which requires the cache coherence control is broadcast to all the nodes requiring the cache coherence control, while the access request not requiring the cache coherence control is transferred only to the node intended as a destination.

9. A node controller included in each node of a shared memory multiprocessor comprising a plurality of nodes each configured with at least one of a processor having a cache memory, a memory device and an I/O device, and a node controller, and an inter-node connection network for interconnecting a plurality of said nodes; wherein at least one of a plurality of said nodes includes said processor and at least one each of said memory device and said I/O device, and the whole of a plurality of said nodes include at least one said processor, at least one said memory device and at least one said I/O device; wherein said node controller of each of a plurality of said nodes includes a processor unit constituting an interface with said processor in the local node, at least one of a memory unit constituting an interface with said memory device in the local node and an I/O unit constituting an interface with said I/O device in the local node, a network unit constituting an interface with said inter-node connection network, and an intra-node connection circuit for connecting said processor unit, at least one of said memory device and said I/O device, and said network unit to each other; wherein said processor unit includes an inter-unit address decode circuit and a cache coherence control circuit, said inter-unit address decode circuit decoding the control information and the address information in said access request, and operating in such a manner that the information on the node associated with the memory unit or the I/O unit intended as an access request destination, the information on the unit intended as an access request destination, and the cache coherence control information indicating whether the cache coherence control is required or not, are added to a memory access request or an I/O access request issued by the processor in the local node said cache coherence control circuit performing the cache coherence control of the processor in the local node in the case where said cache coherence control information added to the access request received from said network unit indicates that the cache coherence control is required; wherein said I/O unit includes an inter-unit address decode circuit for adding the node information and the unit information for the memory unit or the I/O unit intended as an access request destination and the cache coherence control information indicating whether the cache coherence control is required or not, to the memory access request or the I/O access request issued by the I/O device in the local node; wherein said network unit includes a transfer unit for transferring the access request received from said intra-node connection circuit to said inter-node connection network, and a transfer unit for transferring the access request transferred thereto from said inter-node connection network to said intra-node connection network; wherein said intra-node connection circuit includes a route designation circuit for designating the destination of transfer of the access request transferred from said inter-node connection network, based on the cache coherence control information, the node information and the unit information added to said access request, and a transfer unit for transferring said access request to a unit connected to said intra-node connection circuit in response to the designation of said route designation circuit; and wherein that access request issued by said processor or said I/O device which requires the cache coherence control is broadcast to all the nodes requiring the cache coherence control, and the access request not requiring the cache coherence control is transferred only to the node intended as a destination.

13. A shared memory multiprocessor comprising: a plurality of nodes each configured with at least one of a processor having a cache memory, a memory device and an I/O device; and an inter-node connection network for interconnecting a plurality of said nodes; wherein at least one of a plurality of said nodes includes said processor and at least one each of said memory device and said I/O device, and the whole of a plurality of said nodes include at least one said processor, at least one said memory device and at least one said I/O device; wherein each of a plurality of said nodes includes an information adding unit for adding the cache coherence control information indicating whether the cache coherence control is required or not and the node information indicating the node constituting a destination of transfer (destination of access), to the access request issued by said processor or said I/O device in the local node, and outputting the resulting information, and a transfer unit for selectively transferring the access request from said information adding unit to said inter-node connection network; and wherein said inter-node connection network includes a transfer unit which, based on said cache coherence control information and said node information added to the access request, transfers said access request to all the nodes requiring the cache coherence control among a plurality of said nodes in the case where said cache coherence control information indicates that the cache coherence control is required, and transfers said access request only to the node indicated by the node information added to said access request in the case where said cache coherence control information indicates that the cache coherence control is not required.

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L4: Entry 5 of 15 File: USPT Oct 21, 2003

US-PAT-NO: 6636926
DOCUMENT-IDENTIFIER: US 6636926 B2

TITLE: Shared memory multiprocessor performing cache coherence control and node controller therefor

DATE-ISSUED: October 21, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yasuda; Yoshiko	Tokorozawa			JP
Hamanaka; Naoki	Tokyo			JP
Shonai; Toru	Hachioji			JP
Akashi; Hideya	Kunitachi			JP
Tsushima; Yuji	Kokubunji			JP
Uehara; Keitaro	Kokubunji			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03

APPL-NO: 09/ 740816 [PALM]
DATE FILED: December 21, 2000

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	11-366235	December 24, 1999

INT-CL: [07] G06 F 13/00, G06 F 15/167

US-CL-ISSUED: 710/305; 710/317, 711/141, 709/213, 700/5
US-CL-CURRENT: 710/305; 700/5, 709/213, 710/317, 711/141

FIELD-OF-SEARCH: 710/305, 710/317, 710/300, 710/62, 710/4, 710/72, 711/141, 711/148, 711/120, 709/213, 709/214, 709/251, 700/5, 712/14, 712/211

PRIOR-ART-DISCLOSED:

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PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL

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ART-UNIT: 2181

PRIMARY-EXAMINER: Ray; Gopal C.

ABSTRACT:

Each node includes a node controller for decoding the control information and the address information for the access request issued by a processor or an I/O device, generating, based on the result of decoding, the cache coherence control information indicating whether the cache coherence control is required or not, the node information and the unit information for the transfer destination, and adding these information to the access request. An intra-node connection circuit for connecting the units in the node controller holds the cache coherence control information, the node information and the unit information added to the access request. When the cache coherence control information indicates that the cache coherence control is not required and the node information indicates the local node, then the intra-node connection circuit transfers the access request not to the inter-node connection circuit interconnecting the nodes but directly to the unit designated by the unit information.

19 Claims, 16 Drawing figures

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L4: Entry 9 of 15 File: USPT Jul 11, 2000

DOCUMENT-IDENTIFIER: US 6088768 A
TITLE: Method and system for maintaining cache coherence in a multiprocessor-multicache environment having unordered communication

Detailed Description Text (4):
With reference now to the figures and in particular with reference to FIG. 1, there is shown a pictorial representation of a parallel processor or multiprocessor computer system which may be utilized to implement the method and system of the present invention. Such a computer system would contain at least one shared memory 10, at least two caching agents capable of maintaining cached copies from the shared memory, and an interconnect structure 20 between the memory and the cached agents that provides concurrent and unordered transport of communications. The caching agent maintaining the cached copies from the shared memory is typically either a processor with integral cache or an input/output (I/O) device with integral cache. Here, each processor is shown having its own cache, local memory and I/O unit, all connected to a common node.

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L4: Entry 9 of 15 File: USPT Jul 11, 2000

US-PAT-NO: 6088768
DOCUMENT-IDENTIFIER: US 6088768 A

TITLE: Method and system for maintaining cache coherence in a multiprocessor-multicache environment having unordered communication

DATE-ISSUED: July 11, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Baldus; Donald Francis	Mazeppa	MN		
Duffield; Nancy Joan	Rochester	MN		
Hoover; Russell Dean	Rochester	MN		
Willis; John Christopher	Rochester	MN		
Ziegler; Frederick Jacob	Rochester	MN		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 08/ 174648 [PALM]
DATE FILED: December 28, 1993

INT-CL: [07] G06 F 12/00, G06 F 13/00

US-CL-ISSUED: 711/141; 711/118, 711/119, 711/130
US-CL-CURRENT: 711/141; 711/118, 711/119, 711/130

FIELD-OF-SEARCH: 395/471, 395/472, 395/474, 395/477, 395/479, 395/446, 711/3, 711/117, 711/118, 711/119, 711/130, 711/141, 711/154, 711/147

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

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☐	4969146	November 1990	Twitty et al.	370/85.1
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☐				
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☐	5404482	April 1995	Stamm et al.	395/435
☐	5404483	April 1995	Stamm et al.	395/471

ART-UNIT: 272

PRIMARY-EXAMINER: Thai; Tuan V.

ATTY-AGENT-FIRM: Felsman, Bradley, Vaden, Gunter & Dillon, LLP

ABSTRACT:

A method and system for providing cache coherence despite unordered interconnect transport. In a computer system of multiple memory devices or memory units having shared memory and an interconnect characterized by unordered transport, the method comprises sending a request packet over the interconnect from a first memory device to a second memory device requiring that an action be carried out on shared memory held by the second memory device. If the second memory device determines that the shared memory is in a transient state, the second memory device returns the request packet to the first memory device; otherwise, the request is carried out by the second memory device. The first memory device will continue to resend the request packet each time that the request packet is returned.

15 Claims, 4 Drawing figures

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(12) **United States Patent**
Khare et al.

(10) **Patent No.: US 6,772,298 B2**
(45) **Date of Patent: Aug. 3, 2004**

(54) **METHOD AND APPARATUS FOR INVALIDATING A CACHE LINE WITHOUT DATA RETURN IN A MULTI-NODE ARCHITECTURE**

(75) Inventors: **Manoj Khare**, Saratoga, CA (US); **Akhilesh Kumar**, Sunnyvale, CA (US); **Ken Creta**, Gig Harbor, WA (US); **Lily P. Looi**, Portland, OR (US); **Robert T. George**, Austin, TX (US); **Michel Cekleov**, Mountain View, CA (US)

(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 607 days.

(21) Appl. No.: **09/739,667**

(22) Filed: **Dec. 20, 2000**

(65) **Prior Publication Data**

US 2002/0078305 A1 Jun. 20, 2002

(51) **Int. Cl.**[7] **G06F 12/00**

(52) **U.S. Cl.** 711/144; 711/120; 711/141; 711/145; 711/159

(58) **Field of Search** 711/144, 120, 711/141, 145, 159

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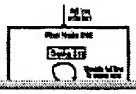
Related U.S. patent application Ser. No. 09/672,454, filed Sep. 29, 2000.
Related U.S. patent application Ser. No. 09/641,708, filed Aug. 21, 2000.

Primary Examiner—Matthew Kim
Assistant Examiner—Stephen Elmore
(74) *Attorney, Agent, or Firm*—Kenyon & Kenyon

(57) **ABSTRACT**

A method of invalidating a cache line in a system having a plurality of nodes that include a processor and a cache memory. A request to invalidate a cache line that is caching a particular memory block is sent from a first node. The request is a request to invalidate a cache line in another node without returning to the first node the data stored in a cache line to be invalidated. In an embodiment, the data in the cache line to be invalidated is not returned to the first node even if the cache line is in the modified state. In a further embodiment, new data is written to a cache line in the first node that is caching the particular memory block without writing old data that was stored in that cache line back to a memory.

19 Claims, 5 Drawing Sheets



US006636926B2

(12) **United States Patent**
Yasuda et al.

(10) **Patent No.: US 6,636,926 B2**
(45) **Date of Patent: Oct. 21, 2003**

(54) **SHARED MEMORY MULTIPROCESSOR PERFORMING CACHE COHERENCE CONTROL AND NODE CONTROLLER THEREFOR**

(75) Inventors: Yoshiko Yasuda, Tokorozawa (JP); Naoki Hamanaka, Tokyo (JP); Toru Shonai, Hachioji (JP); Hideya Akashi, Kunitachi (JP); Yuji Tsushima, Kokubunji (JP); Katsuro Uehara, Kokubunji (JP)

(73) Assignee: Hitachi, Ltd., Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 468 days.

(21) Appl. No.: 09/740,816

(22) Filed: Dec. 21, 2000

(65) Prior Publication Data

US 2001/0005873 A1 Jun. 28, 2001

(30) Foreign Application Priority Data

Dec. 24, 1999 (JP) 11-366235

(51) Int. Cl.[7] G06F 13/00; G06F 15/167

(52) U.S. Cl. 710/305; 710/317; 711/141; 709/213; 700/5

(58) Field of Search 710/305, 317, 710/300, 62, 4, 72; 711/141, 148, 120; 709/213, 214, 251; 700/5; 712/14, 211

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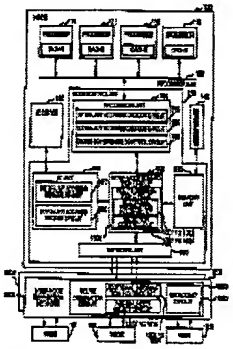
Primary Examiner—Gopal C. Ray

(57) **ABSTRACT**

Each node includes a node controller for decoding the control information and the address information for the access request issued by a processor or an I/O device, generating, based on the result of decoding, the cache coherence control information indicating whether the cache coherence control is required or not, the node information and the unit information for the transfer destination, and adding these information to the access request. An intra-node connection circuit for connecting the units in the node controller holds the cache coherence control information, the node information and the unit information added to the access request. When the cache coherence control information indicates that the cache coherence control is not required and the node information indicates the local node, then the intra-node connection circuit transfers the access request not to the inter-node connection circuit interconnecting the nodes but directly to the unit designated by the unit information.

19 Claims, 12 Drawing Sheets



US-PAT-NO: 6553465

DOCUMENT-IDENTIFIER: US 6553465 B1

TITLE: Multiprocessor system with distributed shared memory having hot plug function for main memories

---------- KWIC ---------

Abstract Text - ABTX (1):

A multiprocessor system of a distributed shared memory structure has a hot plug function for main memories. Each of nodes of the multiprocessor system has a processor, an IO unit, a main memory, a mover, and a routing control unit. If a memory read access request is issued from the processor, the IO unit, or the mover to the main memory of a master node, the routing control unit instructs the master node to transfer the memory read access request. If a memory write access request is issued from the processor, the IO unit, or the mover to the main memory of the master node, the routing control unit instructs both the master node and a slave node to transfer the memory write access request when in a multicasting mode, and instructs only the master node to transfer the memory write access request when not in the multicasting mode.

Claims Text - CLTX (1):

1. A multiprocessor system of a distributed shared memory structure having a plurality of nodes each comprising at least one processor and a main memory, comprising: means for managing the same memory addresses in two nodes; means for holding information of the two nodes as a master node and a slave node; means for transferring a read access request from one of a processor and an I/O unit with respect to said main memory to a master node; a flag indicative of whether a write access request from one of the processor and the I/O unit with respect to said main memory is to be transferred to the master node or to the master node and the slave node; means for transferring the write access request to the master node if said flag indicates that the write access request is to be transferred to the master node; means for transferring the write access request to the master node and the slave node if said flag indicates that the write access request is to be transferred to the master node and the slave node; means for holding address information of a memory space of the main memory of each of the nodes; lock read access means for reading data from

US006553465B1

(12) **United States Patent**
Takusagawa

(10) **Patent No.: US 6,553,465 B1**
(45) **Date of Patent: Apr. 22, 2003**

(54) **MULTIPROCESSOR SYSTEM WITH DISTRIBUTED SHARED MEMORY HAVING HOT PLUG FUNCTION FOR MAIN MEMORIES**

(75) Inventor: **Junichi Takusagawa**, Yamanashi (JP)

(73) Assignee: **NEC Corporation**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/493,241

(22) Filed: Jan. 28, 2000

(30) **Foreign Application Priority Data**

Jan. 28, 1999 (JP) 11-020337

(51) Int. Cl.[7] G06F 12/16

(52) U.S. Cl. 711/152; 711/115; 711/155; 712/31

(58) Field of Search 711/115, 148, 711/152, 153, 165, 170, 162, 155; 712/31; 714/5, 7; 707/10

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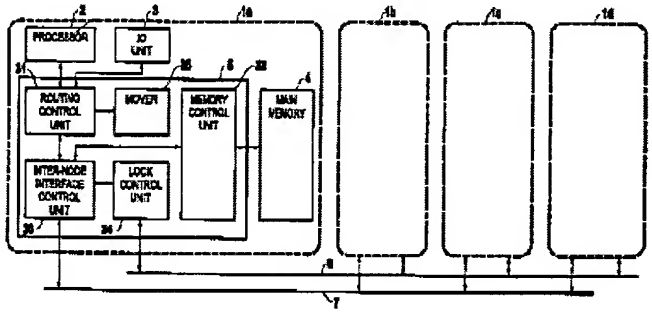
* cited by examiner

Primary Examiner—Gary J Portka
(74) *Attorney, Agent, or Firm*—McGinn & Gibb, PLLC

(57) **ABSTRACT**

A multiprocessor system of a distributed shared memory structure has a hot plug function for main memories. Each of nodes of the multiprocessor system has a processor, an IO unit, a main memory, a mover, and a routing control unit. If a memory read access request is issued from the processor, the IO unit, or the mover to the main memory of a master node, the routing control unit instructs the master node to transfer the memory read access request. If a memory write access request is issued from the processor, the IO unit, or the mover to the main memory of the master node, the routing control unit instructs both the master node and a slave node to transfer the memory write access request when in a multiteasing mode, and instructs only the master node to transfer the memory write access request when not in the multiteasing mode.

7 Claims, 6 Drawing Sheets



US-PAT-NO: 5802578

DOCUMENT-IDENTIFIER: US 5802578 A

TITLE: Multinode computer system with cache for combined tags

---------- KWIC ---------

Abstract Text - ABTX (1):

Local memory on a node in a multinode, multiprocessor computer system with distributed shared memory and a remote cache is efficiently updated through the use of a combined tag stored in a tag cache. In response to a local processor request for access to local memory that does not contain a current copy of the data requested, a combined tag is formed from a memory tag and a remote cache tag. The combined tag allows the node to operate in accordance with the network protocol such as the Scalable Coherent Interface (SCI) while the memory is being updated, acting as memory in response to requests from other nodes to the memory and as a cache in response to requests from other nodes to the remote cache. In this way the memory is updated quickly and the remote cache is not required to store data that is better stored in the local memory.

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 10 of 16 returned.

☐ 1. Document ID: US 6745294 B1

Using default format because multiple data bases are involved.

L4: Entry 1 of 16 File: USPT Jun 1, 2004

US-PAT-NO: 6745294
DOCUMENT-IDENTIFIER: US 6745294 B1

TITLE: Multi-processor computer system with lock driven cache-flushing system

DATE-ISSUED: June 1, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wilson; Kenneth Mark	San Jose	CA		
Pong; Fong	Mountain View	CA		
Russell; Lance	Hollister	CA		
Nguyen; Tung	Cupertino	CA		
Xu; Lu	San Jose	CA		

US-CL-CURRENT: 711/135; 710/200, 711/133, 711/136, 711/141, 711/142, 711/147

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Draw De

☐ 2. Document ID: US 6678799 B2

L4: Entry 2 of 16 File: USPT Jan 13, 2004

US-PAT-NO: 6678799
DOCUMENT-IDENTIFIER: US 6678799 B2

TITLE: Aggregation of cache-updates in a multi-processor, shared-memory system

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Draw De

☐ 3. Document ID: US 6675262 B1

L4: Entry 3 of 16 File: USPT Jan 6, 2004

US-PAT-NO: 6675262
DOCUMENT-IDENTIFIER: US 6675262 B1

h e b b g e e e f e g ef b e

TITLE: Multi-processor computer system with cache-flushing system using memory recall

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Draw De

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☐ 4. Document ID: US 6636949 B2

L4: Entry 4 of 16 File: USPT Oct 21, 2003

US-PAT-NO: 6636949
DOCUMENT-IDENTIFIER: US 6636949 B2

TITLE: System for handling coherence protocol races in a scalable shared memory system based on chip multiprocessing

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Draw De

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☐ 5. Document ID: US 6243794 B1

L4: Entry 5 of 16 File: USPT Jun 5, 2001

US-PAT-NO: 6243794
DOCUMENT-IDENTIFIER: US 6243794 B1

TITLE: Data-processing system with CC-NUMA (cache-coherent, non-uniform memory access) architecture and remote cache incorporated in local memory

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Draw De

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☐ 6. Document ID: US 6141692 A

L4: Entry 6 of 16 File: USPT Oct 31, 2000

US-PAT-NO: 6141692
DOCUMENT-IDENTIFIER: US 6141692 A

TITLE: Directory-based, shared-memory, scaleable multiprocessor computer system having deadlock-free transaction flow sans flow control protocol

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Draw De

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☐ 7. Document ID: US 6058458 A

L4: Entry 7 of 16 File: USPT May 2, 2000

US-PAT-NO: 6058458
DOCUMENT-IDENTIFIER: US 6058458 A

TITLE: Multi-processor system having a shared program memory and related method

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 8. Document ID: US 5875462 A

L4: Entry 8 of 16 File: USPT Feb 23, 1999

US-PAT-NO: 5875462
DOCUMENT-IDENTIFIER: US 5875462 A

TITLE: Multi-processor data processing system with multiple second level caches mapable to all of addressable memory

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 9. Document ID: US 5860108 A

L4: Entry 9 of 16 File: USPT Jan 12, 1999

US-PAT-NO: 5860108
DOCUMENT-IDENTIFIER: US 5860108 A

TITLE: Method and clustered multi-processor system for controlling a clock phase for clusters

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 10. Document ID: US 5802570 A

L4: Entry 10 of 16 File: USPT Sep 1, 1998

US-PAT-NO: 5802570
DOCUMENT-IDENTIFIER: US 5802570 A

TITLE: Multiprocessor system with parallel execution of data

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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Terms	Documents
L1 and L3	16

Display Format: - Change Format

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Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 11 through 16 of 16 returned.

☐ 11. Document ID: US 5752258 A

Using default format because multiple data bases are involved.

L4: Entry 11 of 16 File: USPT May 12, 1998

US-PAT-NO: 5752258
DOCUMENT-IDENTIFIER: US 5752258 A

TITLE: Encoding method for directory state in cache coherent distributed shared memory system

DATE-ISSUED: May 12, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Guzovskiy; Aleksandr	Lowell	MA		
Zak, Jr.; Robert C.	Lexington	MA		
Bromley; Mark	Andover	MA		

US-CL-CURRENT: 711/120; 711/124, 711/145

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 12. Document ID: US 5680571 A

L4: Entry 12 of 16 File: USPT Oct 21, 1997

US-PAT-NO: 5680571
DOCUMENT-IDENTIFIER: US 5680571 A

TITLE: Multi-processor data processing system with multiple, separate instruction and operand second level caches

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 13. Document ID: US 5535116 A

L4: Entry 13 of 16 File: USPT Jul 9, 1996

US-PAT-NO: 5535116
DOCUMENT-IDENTIFIER: US 5535116 A
** See image for Certificate of Correction **

h e b b cg b cc e

TITLE: Flat cache-only multi-processor architectures

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 14. Document ID: US 5530933 A

L4: Entry 14 of 16 File: USPT Jun 25, 1996

US-PAT-NO: 5530933
DOCUMENT-IDENTIFIER: US 5530933 A

TITLE: Multiprocessor system for maintaining cache coherency by checking the coherency in the order of the transactions being issued on the bus

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 15. Document ID: US 5060144 A

L4: Entry 15 of 16 File: USPT Oct 22, 1991

US-PAT-NO: 5060144
DOCUMENT-IDENTIFIER: US 5060144 A

TITLE: Locking control with validity status indication for a multi-host processor system that utilizes a record lock processor and a cache memory for each host processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 16. Document ID: US 4885680 A

L4: Entry 16 of 16 File: USPT Dec 5, 1989

US-PAT-NO: 4885680
DOCUMENT-IDENTIFIER: US 4885680 A

TITLE: Method and apparatus for efficiently handling temporarily cacheable data

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L1 and L3	16

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